IN THE SPECIFICATION:

Please delete the paragraph beginning on page 5, line 20, and replace with the following new paragraph. Changes from the original paragraph are highlighted.

The controller 100 comprises a portion of an integrated circuit device, i.e., an application specific integrated circuit ("ASIC") 150. The ASIC 150 includes a testing interface 180, preferably a Joint Action Test Group ("JTAG") tap controller, through which the BIST of the dual mode BIST controller 100 can be invoked and through which the results may be returned in accordance with conventional practice. The ASIC 150 also includes one or more memory components 190, preferably ~~synchronous~~ static random access memories ("SRAMs"), and combinatorial logic in a plurality of timing domains 195a-d that are tested by the BIST of the dual mode BIST controller 100.

Please delete the paragraph beginning on page 7, line 4, and replace with the following new paragraph. Changes from the original paragraph are highlighted.

One particular embodiment of the LBIST domain 160 is conceptually illustrated in FIG. 2. In this-particular embodiment, the LBIST engine 110 comprises an LBIST state machine 210 and a pattern generator 230. The LBIST domain 160 also includes a multiple input signature register ("MISR") 220. The content of the MISR 220 is the LBIST signature 130 in **FIG. 1.** The pattern generator 230 is, more precisely, a pseudo random pattern generator ("PRPG"). In the illustrated embodiment, the LBIST engine 110 is externally configured by a CONFIGURATION signal with a vector count and a PRPG seed for the pattern generator 230. The LBIST engine 110 is configured by a ~~66-bit~~ 65-bit signal received through the testing interface 180 in which 32 bits contain the vector count and 33 bits contain the PRPG seed. Thus, the pattern generator 230 is programmable, as is the LBIST engine 110 as a whole. However, the invention is not so

limited and other techniques may be employed for configuring the LBIST engine 110. For instance, these values may be hardcoded or hardwired in alternative embodiments.

Please delete the paragraph beginning on page 9, line 20, and replace with the following new paragraph. Changes from the original paragraph are highlighted.

In accordance with yet another aspect of the invention, the content of the LFSR with which the pattern generator 230 is implemented and the register with which the MISR 220 is implemented are generated using different primitive polynomials to prevent failures disguised by aliasing. The content of the LFSR in the illustrated embodiment is based on the 31-bit primitive polynomial $x^{31} + x^3 + 1$ and the content of the MISR 220 is based on the 32-bit primitive polynomial $x^{32} + x^{28} + x + 1$. If the pattern generator 230 enters an all zero state, the error indicator will be activated and stored in bit *B33* of the MISR 220. In this particular embodiment, the even outputs of the LFSR (bits ~~*B26*~~ *B30* *to* B_0) supply the scan pattern to the inputs of the scan chains 1 to 23, respectively. The MISR 220 has inputs that EXCLUSIVEOR into the odd register bits *B7* through *B31* and bit *B0* during the scan operation. Alternative embodiments may omit this aspect of the invention, however.

Please delete the paragraph beginning on page 9, line 32, and replace with the following new paragraph. Changes from the original paragraph are highlighted.

The LBIST engine 110 provides two level sensitive scan device ("LSSD") clocks, shown in **FIG. 9** (LSSD_CLKA and LSSD_CLKB), to the level sensitive scan devices (not shown) in the core 900. Both of these clocks are normally low, but alternately pulse high when the LBIST state machine 210 is in the scan state 330. After the scan chains are flushed, the MISR 220 (shown in FIG. 2) collects the scan data. The LBIST engine 110 also outputs two step clocks LBIST STEP CLKC and LBST STEP ~~STEPE~~ CLKE. The step clock LBIST STEP CLKC actually comprises three signals LBIST STEP CLKC1, LBIST STEP CLKC2, and LBIST STEP CLKC3. The LBST STEP CLKE clock, normally high, enables the LBST STEP CLKC1 through to the core latches (not

shown) *via* the core logic clock splitters (not shown) of the core 900. The LBST STEP CLKC2 is enabled by the LBST STEP CLKE clock through the clock splitters (not shown) of the low power register array ("LPRA") wrappers 905. The LBST STEP CLKE clock also enables the LBST STEP CLKC3 through the clock splitter (not shown) of the wrappers for the memory components ~~150~~ *190, i.e.,* the SRAM wrappers 910.

Please delete the paragraph beginning on page 11, line 14, and replace with the following new paragraph. Changes from the original paragraph are highlighted.

The MBIST engine 120 is therefore modifiable or configurable at the time the ASIC is implemented in a register transfer level ("RTL") specification to accommodate a variety of nested MBIST engines 620 that might be obtained from various vendors. As those in the art having the benefit of this disclosure will appreciate, the nested MBIST engine 620 and the MBIST state machines 610 are ~~a~~ predefined library elements in standard RTL applications software. The RTL specification for the ASIC ~~100~~ 150 contains a logic wrapper (not shown) defining the inputs and outputs for the library elements that define which of the MBIST state machines 610 provides the input and output to the nested MBIST engine 620. The RTL specification is then synthesized into a gate-level implementation for the ASIC ~~100~~ 150.

Please delete the paragraph beginning on page 12, line 26, and replace with the following new paragraph. Changes from the original paragraph are highlighted.

The MBIST state machine 610 transitions to the initialization state 820 upon receipt of a MBIST select signal and a MBIST run signal received through the testing interface 180. The initialization state 820 is followed by a flush and then the test patterns as the MBIST engine 120 cycles through the initialization state 820, flush state 830, and test state 840. This transition occurs upon the completion of initialization of components and signals in the MBIST domain. The flush state 830 continues until the memory components 190 are flushed and initialized ~~them~~ to a known state. The MBIST state machine 610 then transitions to the test state 840. The MBIST engine 120 drives a one

direction test pattern bus (not shown) out to all memory components 190, and they drive the result back to the nested MBIST engine 620 on another direction test pattern bus. The results are stored in the MBIST signature register 605 as part of the MBIST signature 140. When the MBIST is completed, the MBIST state machine 610 transitions to the done state 850, signaling completion by setting the dedicated bit in the MBIST signature register 605 to indicate the MBIST is complete.

Please delete the paragraph beginning on page 13, line 30, and replace with the following new paragraph. Changes from the original paragraph are highlighted.

In operation, the ASIC ~~100~~ 150 shown in **FIG. 1** may be placed on a vendor-supplied tester having a test controller 915 including a JTAG controller 920, shown in **FIG. 9,** typically with several other ASICs 100 (not shown). Alternatively, the ASIC 100 may be tested in a live system having a live system controller 925 including a JTAG controller 920. The MBIST engine 120 includes a MBIST state machine 610, shown in **FIG. 6,** designed for use with this particular vendor-supplied test controller 915. In the illustrated embodiment, the JTAG controller 920 employs JTAG protocols and testing hardware, and so the testing interface 180 is a JTTAP controller. As was noted above, the LBIST and MBIST capabilities of the dual mode BIST controller 100 may be utilized separately or conjunctively. Furthermore, the LBIST and the MBIST may be performed in parallel or in serial. However, the following discussion will contemplate a conjunctive use in serial. It is nevertheless to be understood that only one or the other may be employed in alternative embodiments.